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PTO/SB/08B (08-00)

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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet **3** of **3**

Complete if Known

Application Number	09/802,108
Filing Date	March 8, 2001
First Named Inventor	Saulsbury, Ashley
Group Art Unit	2151
Examiner Name	Unassigned
Attorney Docket Number	016747-017800US

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	AA					
	AB					
	AC					
	AD					

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
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	AF							
	AG							
	AH							

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
WMT	AI	AIMOTO, YOSHIHARU et al.; "A 768GIPS 3.84GB/s 1 W Parallel Image-Processing RAM Integrating a 16 Mb DRAM and 128 Processors"; ISSCC96/Session 23 / DRAM / Paper SP23.3; 1996 IEEE International Solid-State Circuits Conference; pp. 372-373 and 476	
WMT	AJ	BURSKY, DAVE; "Combo RISC CPU and DRAM Solves Data Bandwidth Issues"; Electronic Design; March 4, 1996; pp. 67-71.	
WMT	AK	SAULSBURY, ASHLEY, et al., "Missing the Memory Wall: The Case for Processor/Memory Integration"; ACM; 1996; pp. 90-101	
WMT	AL	SHIMIZU, TORO, et al.; "A Multimedia 32b RISC Microprocessor with 16 Mb DRAM"; ISSCC96/Session 13 / Microprocessors/Paper FP 13.4; 1996 IEEE International Solid State Circuits Conference; pp. 216-217 and 448	
WMT	AM	MITSUBISHI ELECTRIC CORP; Product Specification for Single-Chip 32-Bit CMOS Microprocessor (C16000) 1998	

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Examiner Signature	W. TREAT	Date Considered	4/17/04
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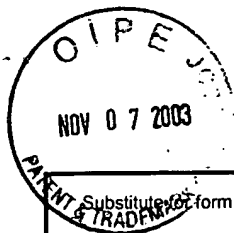
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¹ Unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.

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FORM PTO-1449 (Modified)			Attorney Docket No.: 016747-017800US		Application No.: 09/802,108	
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)			Applicant: Ashley Saulsbury, et al.			
			Filing Date: March 8, 2001		Group: 2151	
Reference Designation			U.S. PATENT DOCUMENTS			Page 1
Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
<u>WMT</u> AA	4,725,945	02/16/88	Kronstadt et al.	364	200	
<u> </u> AB	4,894,770	01/16/90	Ward et al.	364	200	
<u> </u> AC	5,184,320	02/02/93	Dye	365	49	
<u> </u> AD	5,261,066	11/09/93	Jouppi et al.	395	425	
<u> </u> AE	5,317,718	05/31/94	Jouppi	395	425	
<u> </u> AF	5,386,547	01/31/95	Jouppi	395	425	
<u> </u> AG	5,564,035	10/08/96	Lai	395	471	
<u> </u> AH	5,588,130	12/24/96	Fujishima et al.	395	445	
<u> </u> AI	5,623,627	04/22/97	Witt	395	449	
<u> </u> AJ	5,649,154	07/15/97	Kumar et al.	395	449	
<u> </u> AK	5,650,955	07/22/97	Puar et al.	365	51	
<u> </u> AL	5,687,338	11/11/97	Boggs et al.	395	381	
<u> </u> AM	5,703,806	12/30/97	Puar et al.	365	181	
<u> </u> AN	5,900,011	05/04/99	Saulsbury et al.	711	119	
<u>WMT</u> AO	6,128,702	10/03/00	Saulsbury et al.	711	133	
FOREIGN PATENT DOCUMENTS						
	Document No.	Date	Country	Class	Sub-class	Translation (Yes/No)
<u> </u> AP						
<u> </u> AQ						
<u> </u> AR						
<u> </u> AS						
<u> </u> AT						
<u> </u> AU						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
<u> </u> AV						
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<u> </u> AX						
<u> </u> AY						
<u> </u> AZ						
EXAMINER	<u>W. TREAT</u>		DATE CONSIDERED	<u>4/17/04</u>		

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Substitute for form 1449A/PTO			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Application Number	09/802,108
			Filing Date	March 8, 2001
			First Named Inventor	Saulsbury, Ashley
			Art Unit	2151
			Examiner Name	Unassigned
Sheet	1	of	Attorney Docket Number	016747-017800US

U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
WMT	AA	US-4,980-819	12/1990	Cushing et al.	RECEIVED NOV 10 2003 Technology Center 2100
	AB	US-5,301,340	4/1994	Cook	
	AC	US-5,530,817	6/1996	Masubuchi	
	AD	US-5,710,907	1/1998	Hagersten et al.	
	AE	US-5,953,738	9/1999	Rao	
	AF	US-6,000,007	12/1999	Leung et al.	
	AG	US-6,128,700	10/2000	Hsu et al.	
	AH	US-6,202,143	3/2001	Rim	
	AI	US-6,256,256	7/2001	Rao	
	AJ	US-6,275,900	8/2001	Liberty	
WMT	AK	US-6,321,318	11/2001	Baltz et al.	
	AL	US-			
	AM	US-			
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		Country Code ³	Number ⁴ Kind Code ⁵ (if known)				
WMT	AU	PCT	WO 00/33178	6/8/2000	Sun Microsystems, Inc.		<input type="checkbox"/>
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	AW						<input type="checkbox"/>
	AX						<input type="checkbox"/>
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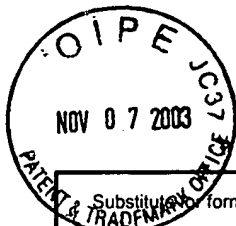
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		Filing Date	March 8, 2001		
		First Named Inventor	Saulsbury, Ashley		
		Art Unit	2151		
		Examiner Name	Unassigned		
Sheet	2	of		Attorney Docket Number	016747-017800US

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
WMT	BC	NUMOMURA Y ET AL: "M32R/D-INTEGRATING DRAM AND MICROPROCESSOR" IEEE MICRO, IEEE INC. NEW YORK, US, vol. 17 no. 6, 1 November 1997 (1997-11-01), pages 40-48, XP000726003; ISSN: 0272-1732.	
WMT	BD	KOZYRAKIS C E ET AL: "SCALABLE PROCESSORS IN THE BILLION-TRANSISTOR ERA: IRAM" COMPUTER, IEEE COMPUTER SOCIETY, LONG BEACH., CA, US, US vol. 20, no. 0 1 September 1997 (1997-09-01), pages 75-78, XP000730003; ISSN: 0018-9162.	
WMT	BE	HERRMANN KLAUS, HILGENSTOCK JOERG, PIRSCH PETER: "ARCHITECTURE OF A MULTIPROCESSOR SYSTEM WITH EMBEDDED DRAM FOR LARGE AREA INTEGRATION" 8 October 1997 (1997-10-08), IEEE INTERNATIONAL CONFERENCE ON INNOVATIVE SYSTEMS IN SILICON, PISCATAWAY, NJ, USA; XP002179990	
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Examiner Signature	W. TREAT	Date Considered	4/17/04
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